TRANSIENT CAPLESS ANNEALING OF ION-IMPLANTED PBN LEC GaAs FOR MONOLITHIC MICROWAVE INTEGRATED CIRCUITS

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ABSTRACT

A method for high-temperature, capless activation of implanted gallium arsenide has been devised based on the recent availability of high-purity semi-insulating PBN LEC gallium arsenide[1] both as implant host and stabilizing medium.

This new capless technology, "Transient Capless Annealing," has shown high activation of implanted dose (85%) with high uniformity (±4.5%) and abrupt (500Å/decade) carrier concentration depth profiles at 1.5×10^{17} cm^{-3} doping. Hall measurements taken from activated films show an electron mobility of 4500 cm^2/volt-sec at room temperature with less than 1000Å Schottky barrier surface depletion depth.

S-band integrated circuits fabricated by transient capless annealing of discretely implanted $^{29}Si^+$ delivered 20 dB of gain and 29 dBm of output power between 3.0 and 3.6 GHz.

The high-throughput, batch-processing nature of transient capless annealing makes this process commercially attractive for high-yield, integrated circuit production in gallium arsenide.

INTRODUCTION

Direct ion implantation of doping species into semi-insulating wafers of gallium arsenide followed by thermal annealing and activation has been demonstrated as a viable technique in the preparation of several electronic devices, in particular Field Effect Transistors (FETs),[2] injection lasers,[3] and monolithic integrated circuits[4] using a variety of capped and capless activation technologies.

For successful FET and integrated circuit fabrication, the annealing and activation process should possess the following features:

1. High activation of implanted dose,
2. Wide range of available activated dopant concentration,
3. Uniform activation of dose across large-area wafers,
4. Precise and predictable net donor density,
5. Near theoretical electron mobility,
6. Negligible surface compensation,
7. Sharp and abrupt profile shape,
8. Simultaneous multiple implant activation,
9. Large-area wafer capacity (2- and 3-inch diameter),
10. Large-volume batch production,
11. Flat, mirror-like and damage-free wafer surfaces, and
12. Low dielectric loss regions between discrete implants.

This paper is intended to show that "transient capless annealing" of implants into PBN LEC substrates can meet these stringent requirements for FET and IC production.

IMPLANT ACTIVATION BY THERMAL ANNEALING

The minimum temperature for substantial implant activation in GaAs is between 750°C and 800°C. This high temperature is necessary in order to anneal damage present in the gallium arsenide lattice caused by the penetration of high-energy ions, and to move the implanted ions to electrically active, substitutional sites. Straightforward heating of an implanted GaAs wafer to the activation temperature suffers from two drawbacks. First, the vapor pressure of gallium arsenide is substantial in this temperature range,[5] so that the gallium arsenide surface is eroded; secondly, the evaporation is not congruent, so that the arsenic and gallium losses are not equal. From the vapor pressure/temperature diagram for gallium arsenide shown in Figure 1a, it is clear that any temperature above the congruent evaporation temperature (650°C) that might be used to activate an implant will result in incongruent loss of the wafer surface. Figure 2 is a micrograph of the surface of a gallium arsenide (100) wafer that was heated to 900°C in dry hydrogen. The result of incongruent wafer loss is evident as surface roughness and a substantial arsenic vacancy concentration.

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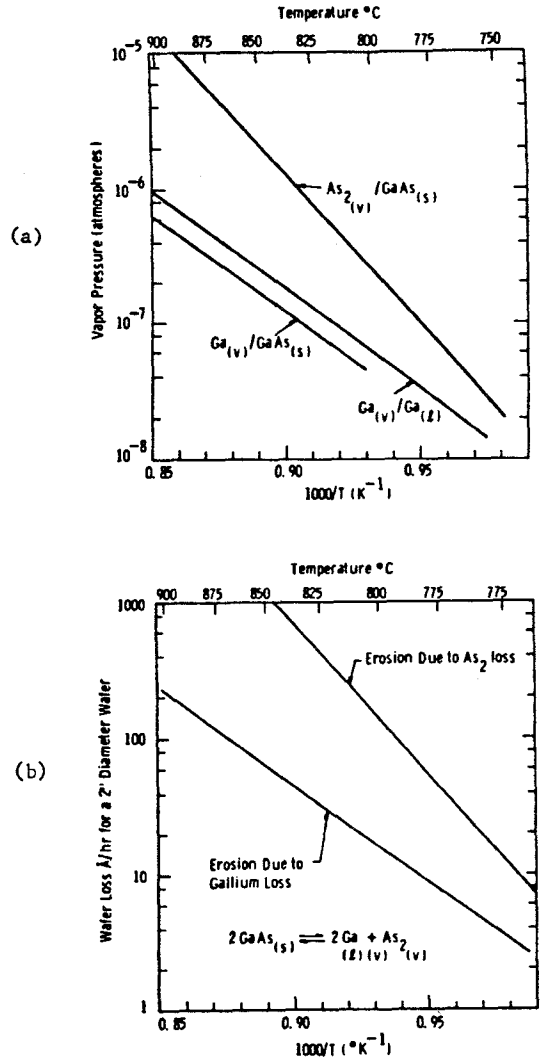

Figure 1. Both a gallium and an arsenic pressure are present over gallium arsenide solid in the annealing temperature range. (a) the pressure of gallium and arsenic over GaAs against temperature; (b) erosion rate for a 2-inch diameter gallium arsenide wafer is shown against temperature.

TRANSIENT CAPLESS ANNEALING

This technology was evaluated using 2- and 3-inch diameter (100) PBN LEC wafers implanted directly with $^{29}Si^{+}$ at ambient temperature, using ion energies of 20 KeV to 800 KeV at doses calculated by LSS theory, to achieve doping densities of 3×10^{16} cm^{-3} to 3×10^{19} cm^{-3}. An angle of 7^{o} to the ion implant beam was employed to reduce channeling effects.

Annealing was performed in a silica tube containing a boat filled with crushed high-purity (PBN LEC) gallium arsenide solid. The slight decomposition of the crushed solid creates both a gallium and an arsenic pressure in the system greater than the decomposition pressure of the implanted wafers by virtue of a temperature differential. Figure 3 shows a schematic diagram of the annealing furnace and reaction chambers. The implanted wafers suffered no observable degradation of surface quality or of electrical behavior as a result of the high-temperature implant activation process.

Figure 4 shows the unloading of twelve 2-inch diameter activated wafers from the anneal zone of the transient capless anneal tube and demonstrates the high-volume batch capability of the process and the highly reflective mirror finish of the wafers.

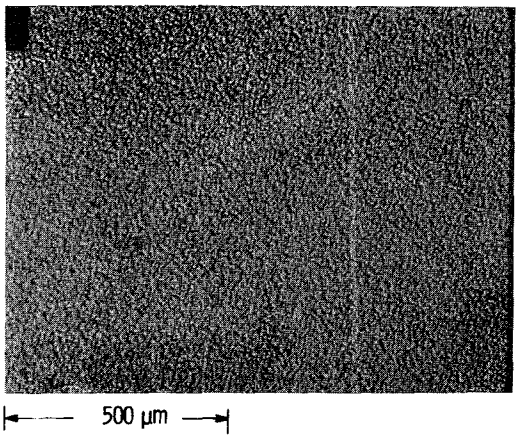

Figure 2. A micrograph of a gallium arsenide wafer that was subjected to high-temperature erosion.

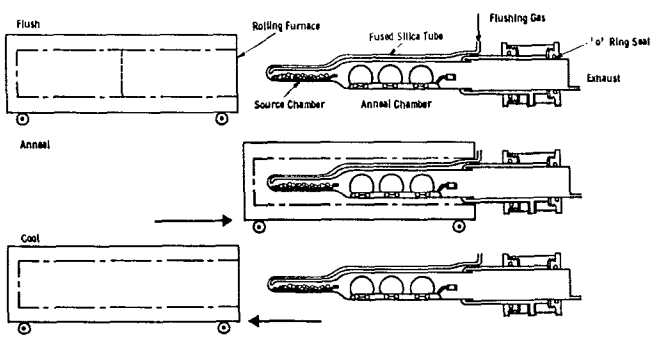

Figure 3 Crushed PBN LEC solid is loaded into the source chamber and implanted wafers are loaded into the anneal chamber of the transient capless anneal tube.

Electrical Assessment

Uniform activated implants were characterized for their differential activation, carrier mobility, and compensation ratio by the use of Hall data. Cloverleaf Van der Pauw samples were cut from the wafers and alloyed tin dots were used to make electrical contact. Information concerning peak electron density, profile shape and depth, and wafer uniformity was obtained from

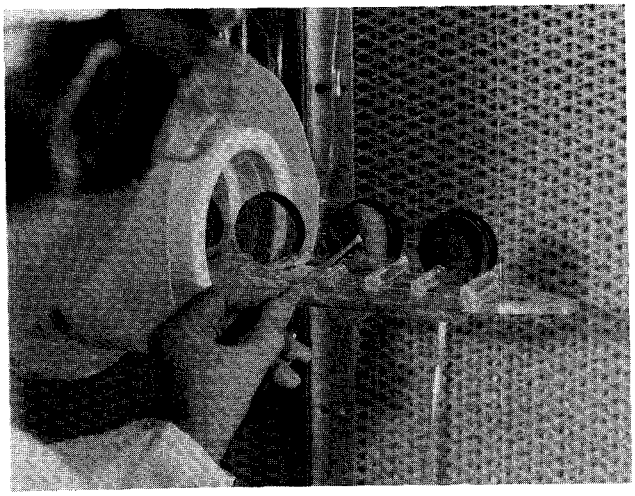

Figure 4. After transient capless annealing the twelve 2-inch diameter wafers are removed from the reaction chamber for electrical assessment and device fabrication.

surface patterns of aluminum dots evaluated with the use of a C-V profiler.

In Figure 5 the observed electrically active impurity density for transient capless anneals is plotted against the implanted ion density for $^{29}Si^{+}$. The total ionized impurity density was deduced from room temperature Hall data and theoretical compensation curves.[6]

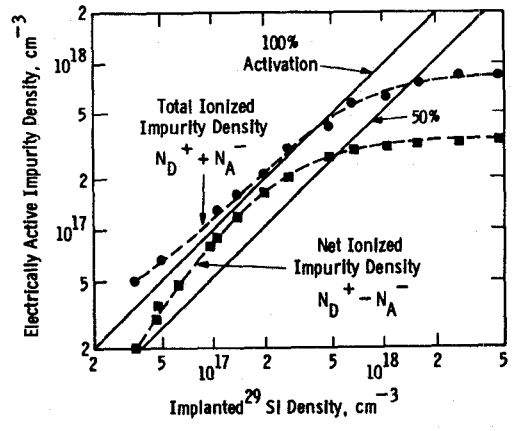

Figure 5. A plot of implanted ion density against ionized impurity density reveals information concerning differential activation, compensation ratio, and background impurity contributions.

This analysis allows evaluation of both the ionized donor and ionized acceptor densities. Saturation of the net donor density and the total ionized center density at high implanted Si concentration may be explained as the exhaustion of the gallium vacancies required to achieve substitutional doping, e.g.

$$Si + V_{Ga} \rightarrow [Si]_{Ga} \quad (1)$$

For doping densities of greatest interest ($n = N_D^+ - N_A^- \leq 2 \times 10^{17}$ cm^{-3}), the activation may be modeled by two linear equations:

$$N_D^+ + N_A^- = [Si] + 1.5 \times 10^{16} \text{ cm}^{-3} \quad (2)$$

and

$$N_D^+ - N_A^- = 0.86\,[Si] - 1.5 \times 10^{16} \text{ cm}^{-3}, \quad (3)$$

which can be solved to give

$$N_D^+ = 0.93\,[Si] \quad (4)$$

and

$$N_A^- = 0.07\,[Si] + 1.5\ 10^{16} \text{ cm}^{-3}. \quad (5)$$

Activation of the implanted dopant is, therefore, assumed to be complete, with 93% of the implanted Si acting as donors and 7% as acceptors. The divergence of the logarithmic density curves at low concentrations is strong evidence for an inherent residual acceptor density of 1.5×10^{16} cm^{-3} in PBN LEC substrate wafers. This residual acceptor usefully preserves the semi-insulating nature of unimplanted regions of the wafer throughout the annealing and activation cycle.

Further information about this low background compensation is given by the room temperature electron mobility curves of Figure 6, where a

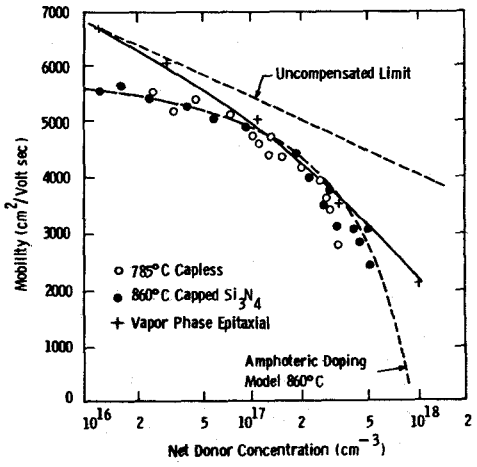

Figure 6. Net donor density is plotted against mobility for capped and capless activations in PBN LEC GaAs wafers. Theoretical and epitaxial results are given for comparison.

comparison is made between capped, capless, and epitaxially produced films. Throughout the range 10^{16} cm^{-3} to 5 x 10^{17} cm^{-3} the capped and capless data are equivalent, both showing the presence of a compensating impurity below 5 x 10^{16} cm^{-3} net donor concentration when compared to epitaxial and theoretical results. In the range of particular interest for FETs and ICs between 5 x 10^{16} cm^{-3} and 3 x 10^{17} cm^{-3}, the room temperature electron mobility of transient capless-annealed implants compared favorably with observed data from epitaxially deposited films.

As indicated in Figure 7, the activation of $^{29}Si^{+}$ in PBN LEC GaAs by transient capless annealing is most uniform. Aluminum dots were evaporated on a 2-inch diameter capless-activated wafer and the peak carrier concentration was determined beneath each dot. Of 300 measurements, the average peak carrier concentration was 7.76 x 10^{16} cm^{-3} and the standard deviation was 4.5%.

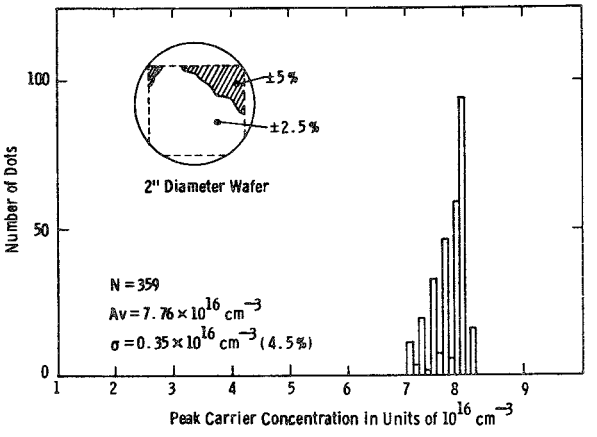

Figure 7. Aluminum Schottky barrier dots reveal the uniformity of transient capless-annealed profiles in PBN LEC gallium arsenide; of 369 dots, the average peak carrier concentration is 7.76 x 10^{16} cm^{-3} and the standard deviation is 0.35 x 10^{16} cm^{-3}.

ELECTRONIC DEVICE STRUCTURES

Transient capless annealing has been used to fabricate various profiles for electronic devices such as the X-band FET, X-band power IC, S-band cascode, power FET, and S-band phase shifter, which were each prepared by the simultaneous activation of multiple implants. Examples of the carrier concentration-depth profiles of such activated implants are shown in Figure 8.

These data illustrate the flexibility of the implant and anneal approach.

FETs AND INTEGRATED CIRCUITS

A two-stage monolithic S-band GaAs power amplifier, designed as the driver in a phased-array T/R module, has been fabricated and tested.

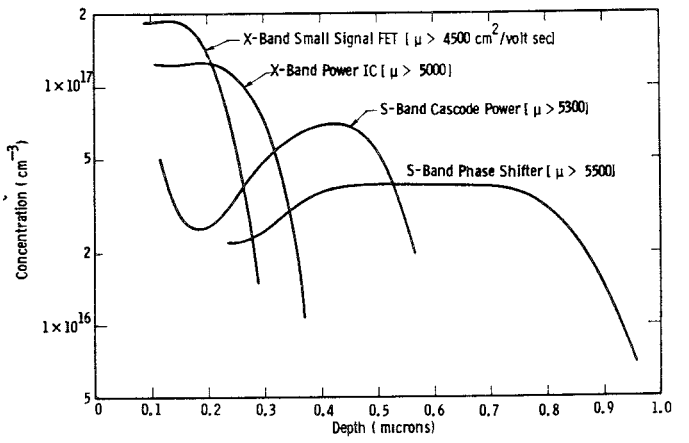

Figure 8. Various electronic device profiles fabricated in PBN LEC gallium arsenide by implantation and transient capless activation.

The amplifier consisted of a 1200 μm FET in the first stage and a 2400 μm FET in the second stage. The circuit contained interdigital capacitors and microstrips for low-loss impedance matching, DC voltage blocking, power splitting, and power combining.

Selectively implanted FET channel layers (N_D = 1.5 x 10^{17} cm^{-3} λ = 3000 Å) were formed by directly implanting ^{29}Si into undoped LEC semi-insulating GaAs substrates through a photoresist mask. Registration marks were then made by a self-aligned method and activation was accomplished by transient capless annealing. After implant characterization, IC fabrication was achieved using AuGe/Ni/Pt ohmics, 1 μ long Ti/Pt/Au gates, interdigital capacitors, plated Au circuits, air-bridge interconnects, and via-hole grounding through 4 mil thick substrates. Two of these completed S-band driver circuits are shown in Figure 9.

The 1200 μm FETs demonstrated a DC transconductance of 120 ms at zero gate bias and a gate drain breakdown voltage near pinchoff in excess of 20 volts for an I_{DSS} of 330 mA. The variation of I_{DSS} over a 2-inch wafer was less than 6%. During RF power testing the two-stage amplifiers delivered 20 dB of gain and 29 dBm of output power in the 3.0 to 3.6 GHz frequency range. A three-dimensional plot of gain, frequency, and power performance of an S-band driver chip is shown in Figure 10.

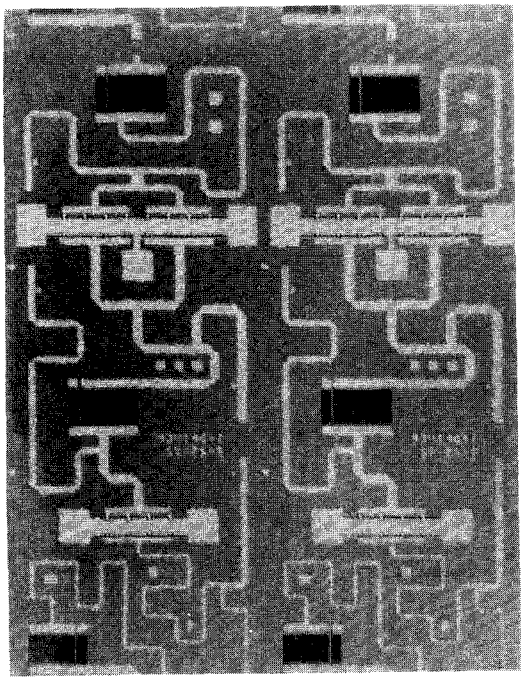

Figure 9. A micrograph of the S-band integrated circuit chip showing airbridges and interdigitated capacitors.

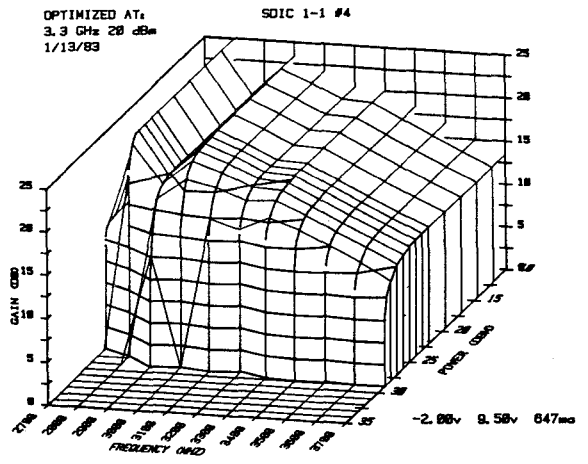

Figure 10. A 3-D plot of gain-power-frequency for the S-band circuit of Figure 9.

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